

In the Claims

Amend claims 1, 5, 8, 17, 19, 21 and 22 as follows:

1. (currently amended) A method of fabricating a MIM capacitor comprising:
providing a semiconductor wafer; and
~~on a semiconductor wafer comprising~~ depositing semi-transparent metal layers for top
and bottom electrodes of said MIM capacitor, ~~said method comprising~~using a two-
mask process for direct alignment;
said method and eliminating the need for alignment trenches in an insulating or oxide
layer.
2. (original) The method of claim 1 wherein said metal layers comprise a low
resistance, high transmittance metal.
3. (original) The method of claim 1 wherein said semi-transparent metal layers are at
least transparent in a portion of the visible spectrum.
4. (original) The method of claim 1 wherein said semi-transparent metal layers comprise
indium-tin-oxide.
5. (currently amended) A method of fabricating a MIM capacitor comprising:
~~The method of claim 1 further comprising:~~

providing a semiconductor wafer;

depositing semi-transparent metal layers on said semiconductor wafer for top and bottom electrodes of said MIM capacitor using a two-mask process for direct alignment and eliminating the need for alignment trenches in an insulating or oxide layer;

depositing a layer of dielectric material between said semi-transparent metal layers;

patterning and etching said top and bottom electrodes from said dielectric material and said semi-transparent metal layers, such that said bottom electrode aligns to a previous metal interconnect layer;

depositing an interlayer dielectric over said top and bottom electrodes;

forming lines through said interlayer dielectric to said top and bottom electrodes; and

depositing a metal liner and metal fill in said lines.

6. (original) The method of claim 5 further comprising planarizing said interlayer dielectric.

7. (original) The method of claim 5 further comprising chemical-mechanical polishing said MIM capacitor after depositing said metal liner and metal fill.

8. (currently amended) A method of fabricating a MIM capacitor on a semiconductor wafer having an insulating layer thereon, said method comprising:

providing said semiconductor wafer having said insulating layer thereon;

depositing alternate layers of a dielectric material and a semi-transparent metal on said insulating layer;

patterning and etching said dielectric layer and said semi-transparent metal layer to form a top electrode;

performing direct alignment to a previous metal interconnect layer through said semi-transparent metal layer;

patterning and etching said capacitor dielectric layer and said semi-transparent metal layer to form a bottom electrode;

depositing an oxide interlayer dielectric over said top and bottom electrodes;

patterning and etching said oxide interlayer dielectric to form lines to said top and bottom electrodes; and

depositing a metal liner and metal fill in said lines.

9. (original) The method of claim 8 wherein said semi-transparent metal comprises a low resistance, high transmittance metal, at least semi-transparent in a portion of the visible spectrum.

10. (original) The method of claim 8 wherein said semi-transparent metal comprises indium-tin-oxide.

11. (original) The method of claim 8 wherein said capacitor dielectric comprises SiNx.

12. (original) The method of claim 8 further comprising planarizing said interlayer dielectric after depositing said interlayer dielectric.

13. (original) The method of claim 8 further comprising removing excessive conductive material by chemical-mechanical polishing after depositing said metal liner and metal fill deposition.

14. (original) The method of claim 8 wherein said patterning comprises applying a photoresist mask and developing said mask with ultraviolet light.

15. (original) The method of claim 8 wherein said etching comprises performing reactive ion etching.

16. (original) The method of claim 10 further comprising indium-tin-oxide metal having a resistivity in the range of 230 mohm-cm after exposure to an annealing temperature of approximately 250°C in a N₂H₂ atmosphere.

17. (currently amended) A method of fabricating a thin film resistor ~~on a semiconductor wafer comprising:~~

providing a semiconductor wafer; and

depositing semi-transparent resistor material on said semiconductor wafer, using said semi-transparent resistor material to eliminate a mask alignment process step.

18. (original) The method of claim 17 wherein said semi-transparent resistor material is indium-tin-oxide, or other metallic material at least transparent in a portion of the visible spectrum.

19. (currently amended) A method of fabricating a thin film resistor comprising: ~~The method of claim 17 further comprising:~~

providing a semiconductor wafer;

depositing a SiNx cap layer over an interconnect copper layer;

depositing a layer of semi-transparent resistor material over said SiNx cap; and

patterning and etching said semi-transparent resistor material with a photoresist mask,
such that said resistor material aligns to said interconnect copper layer.

20. (original) The method of claim 19 wherein said resistor material is indium-tin-oxide, or other metallic material at least transparent in a portion of the visible spectrum.

21. (currently amended) A method of fabricating a MIM capacitor ~~on a semiconductor wafer having an insulating layer thereon~~, said method comprising:

providing a semiconductor wafer having an insulating layer thereon;

depositing alternate layers of a dielectric material and a semi-transparent metal on said insulating layer, wherein said semi-transparent metal comprises indium-tin-oxide

having a resistivity in the range of 230 mohm-cm after exposure to an annealing temperature of approximately 250°C in a N₂H₂ atmosphere;

patterning and etching said dielectric layer and said semi-transparent metal layer to form a top electrode;

patterning and etching said capacitor dielectric layer and said semi-transparent metal layer to form a bottom electrode, such that said bottom electrode aligns to a previous metal interconnect layer;

depositing an oxide interlayer dielectric over said top and bottom electrodes;

patterning and etching said oxide interlayer dielectric to form lines to said top and bottom electrodes; and

depositing a metal liner and metal fill in said lines.

22. (currently amended) A method of fabricating a thin film resistor ~~on a semiconductor wafer comprising:~~

providing a semiconductor wafer;

depositing a SiNx cap layer over an interconnect copper layer on said semiconductor wafer;

depositing a layer of semi-transparent resistor material over said SiNx cap to eliminate a mask alignment process step; and

patterning and etching said semi-transparent resistor material with a photoresist mask, such that said resistor material aligns to said interconnect copper layer.

23. (previously presented) The method of claim 22 wherein said resistor material is indium-tin-oxide, or other metallic material at least transparent in a portion of the visible spectrum.